Listing of the Claims

1. (currently amended) A heterostructure containing ~~the~~ semiconductor alloys ~~$Ga_xIn_{1-x}As$ and $InAs_yP_{1-y}$~~ for minimizing dislocations resulting from lattice mismatch of an active, heteroepitaxial layer, the heterostructure comprising:

a substrate;

a compositionally graded region terminated by a strained buffer layer;

a relaxed intermediate region;

an active layer, wherein a lattice constant of the buffer layer parallel to the substrate is matched to a lattice constant of the relaxed intermediate region to discourage glide of threading dislocations from the strained buffer layer to the active layer; and

a capping layer.

2. (original) The heterostructure of claim 1 wherein the substrate is constructed from InP.

3. (previously presented) The heterostructure of claim 1 wherein the graded region is constructed from $InAs_yP_{1-y}$.

4. (previously presented) The heterostructure of claim 3 wherein the composition within the $InAs_yP_{1-y}$ graded region is varied incrementally thereby accommodating the mismatch of the active layer.

5. (previously presented) The heterostructure of claim 1 wherein the buffer layer is a strained buffer layer constructed from $InAs_yP_{1-y}$.

6. (original) The heterostructure of claim 5 wherein the strained $InAs_yP_{1-y}$ buffer layer is grown to a thickness of approximately one (1) μm.

7. (original) The heterostructure of claim 1 wherein the active layer is constructed from $Ga_xIn_{1-x}As$.

8. (original) The heterostructure of claim 7 wherein the $Ga_xIn_{1-x}As$ active layer is deposited upon the buffer layer.

9. (original) The heterostructure of claim 1 wherein the capping layer is constructed from $InAs_yP_{1-y}$.

10. (original) The heterostructure of claim 9 wherein the $InAs_yP_{1-y}$ capping layer is grown for electrical passivation.

11. (previously presented) The heterostructure of claim 1 wherein the active layer is constructed from epitaxial $Ga_xIn_{1-x}As$ with $x<0.47$, and the graded region and buffer layer are constructed from $InAs_yP_{1-y}$.

12. (original) The heterostructure of claim 1 wherein each of the layers is deposited with a vapor-phase epitaxy technique.

13. (currently amended) A method for eliminating strain and dislocations resulting from lattice mismatch of a heteroepitaxial layer, the method comprising:

providing a substrate;

depositing a compositionally graded region on the substrate;

terminating the graded region with a buffer layer;

depositing a relaxed intermediate region on the buffer layer;

depositing an active layer on the relaxed intermediate region, such that a lattice constant of the buffer layer parallel to the substrate is matched to a lattice constant of the relaxed intermediate region to discourage glide of threading dislocations from the strained buffer layer to the active layer; and

depositing a capping layer on the active layer.

14. (original) The method of claim 13 further comprising: constructing the substrate from InP.

15. (previously presented) The method of claim 13 further comprising: constructing the graded layer from $InAs_yP_{1-y}$.

16. (previously presented) The method of claim 15 further comprising: incrementally varying the composition y of the graded layer thereby accommodating the mismatch of the heteroepitaxial layer.

17. (original) The method of claim 13 further comprising: constructing the a strained buffer layer from $InAs_yP_{1-y}$.

18. (original) The method of claim 17 further comprising: growing the strained $InAs_yP_{1-y}$ buffer layer to a thickness of approximately one (1) μm.

19. (original) The method of claim 13 further comprising: constructing the active layer from $Ga_xIn_{1-x}As$.

20. (original) The method of claim 19 further comprising: depositing the $Ga_xIn_{1-x}As$ active layer upon the buffer layer.

21. (original) The method of claim 13 further comprising: constructing the capping layer from of $InAs_yP_{1-y}$.

22. (original) The method of claim 21 further comprising: growing the $InAs_yP_{1-y}$ capping layer for electrical passivation.

23. (original) The method of claim 13 further comprising: depositing each layer by vapor-phase epitaxy.

24. (previously presented) The heterostructure of claim 1 wherein the graded region is step-graded.

25. (previously presented) The heterostructure of claim 1 wherein substrate is semi-insulating.

26. (currently amended) The heterostructure of claim 1 wherein the buffer layer is a compositional overshoot which compensates for residual strain in the buffer layer such that the lattice constant in a growth ~~plain~~ plane matches that of the relaxed lattice constant of both the intermediate region and the active layer.

27. (previously presented) The heterostructure of claim 1 wherein the intermediate region includes at least one displacement layer.

28. (previously presented) The method of claim 13 wherein the graded region is step-graded.

29. (previously presented) The method of claim 13 wherein the substrate is semi-insulating.

30. (currently amended) The method of claim 13 wherein the buffer layer is a compositional overshoot which compensates for residual strain in the buffer layer such that the lattice constant in a growth ~~plain~~ plane matches that of the relaxed lattice constant of both the intermediate region and the active layer.